CSC Muon Trigger Overview

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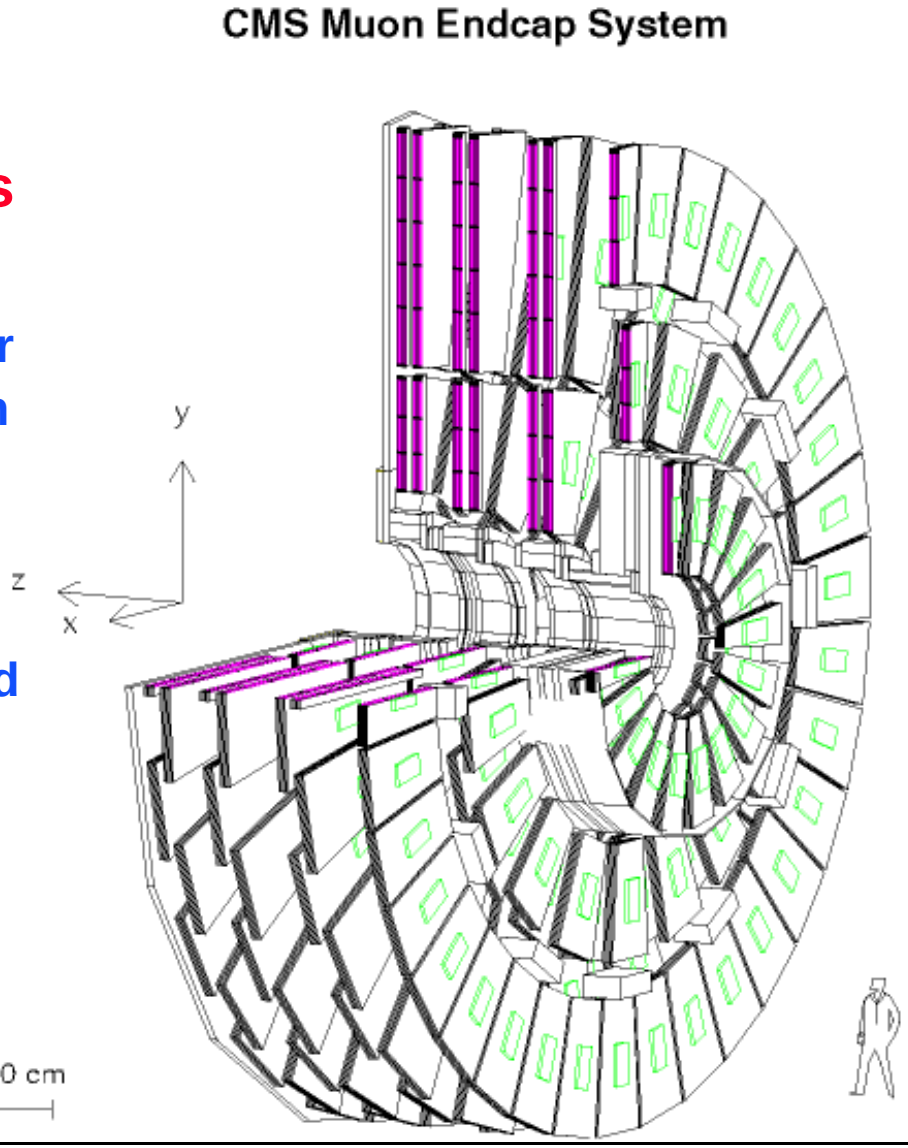
Talk Outline

- ***Brief*** **technical overview of the CSC muon trigger**
- **Progress thus far**
- **Remaining technical issues**
- **Project status**

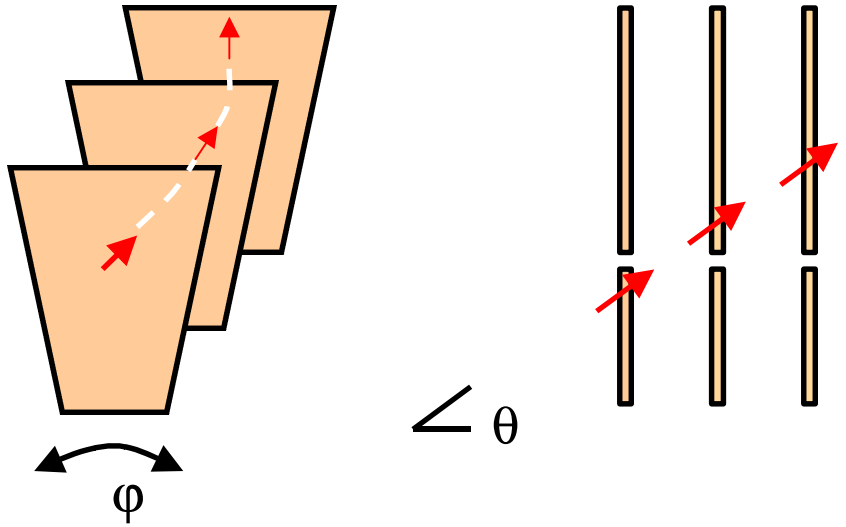
CMS Endcap Muon System

- 3 or 4 stations
- Each CSC chamber has six planes:
  1. Radial cathode strips for precision muon position and bend direction measurement
  2. Anode wires for timing (bunch ID) and non-bend position measurement

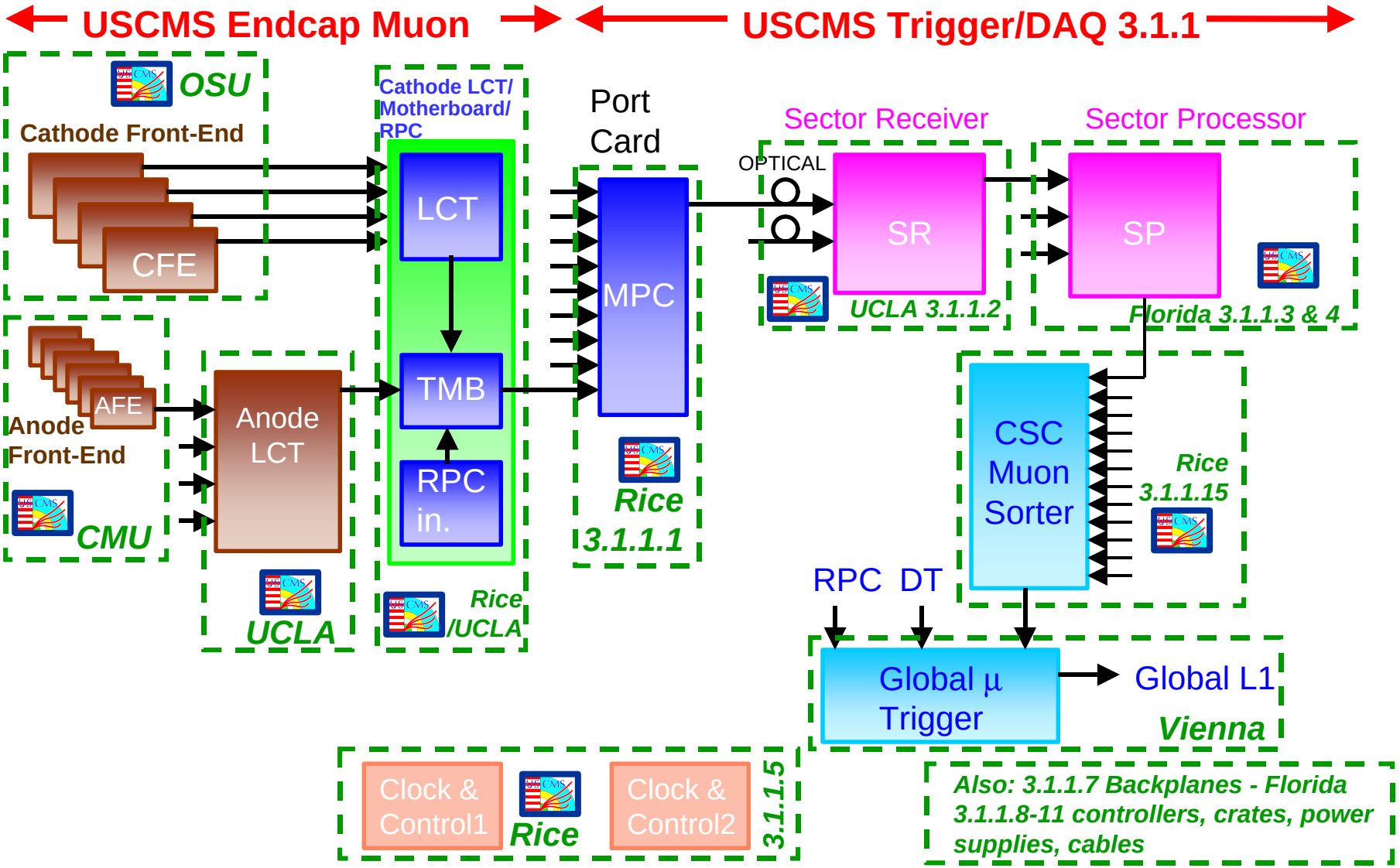


CSC Muon Triggering

- **Trigger primitives are wire and strip segments**
  - Wires give 25ns bunch crossing
  - Strips give precision φ information
- **Link trigger primitives into tracks**
- **Assign p_T, j , and h**
- **Send highest quality tracks to Global L1**



Responsibilities



Current Project Status

- **(Trigger primitives are formally part of Endcap Muon project**
  - **Several rounds of prototyping and test beams done**
  - **On-chamber electronics: production starting soon**
  - **Off-chamber electronics: production following year)**

- **First Track Finder system (TRIDAS) prototyped successfully last year**
  - **Also, trigger part of CMS OO simulation package has been developed**
  - **Some hardware modifications are desired:**
    - Decrease latency
    - Implement DAQ diagnostic readout

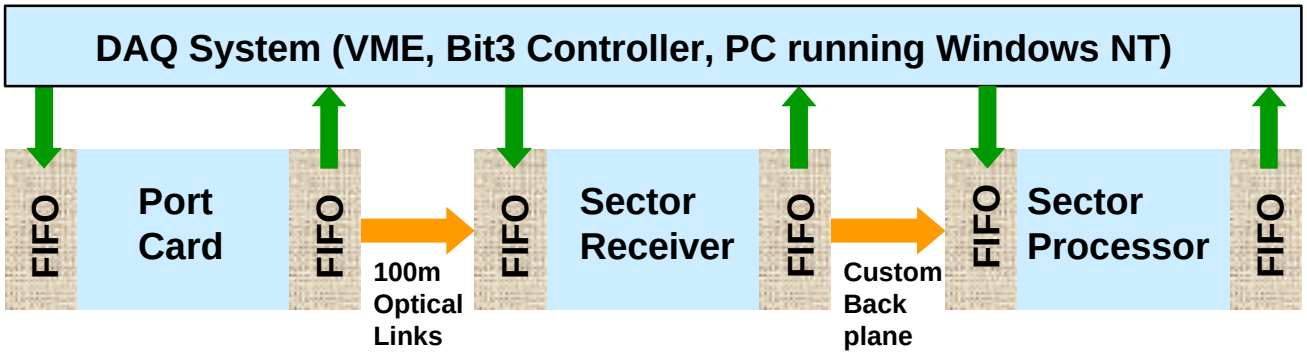
- **Present and future activities**
  - **Last 6 months: R&D on optical links, FPGA logic, memory look-ups, backplane technology, and DAQ readout**
  - **Will need to build a CSC Muon Sorter module as well**
  - **Planning for 2nd prototype round is under discussion**

Track Finder Prototype

✓ **FY 2000 focus was on producing and testing a Track Finder prototype during summer:**

Items produced:

- Backplane (Florida)
- Sector Processor (Florida)
- Muon Port Card (Rice)
- Clock and Control Board (Rice)
- Sector Receiver (UCLA)
- Test software support (all)



✓ **Results included in Trigger TDR (Oct. 2000):**

- > Input data bits loaded into Port Card or SR
- > Data clocked through MPC SR SP at full speed
- > Results examined for validity

Technical Issues (I)

- **Level 1 trigger latency**
  - **Front-end buffer size is limited (tracking, pre-radiators)**
  - **Track Finder must deliver muons to GMT by 79 crossings (1975 ns) after muon collision**
  - **Present prototypes (including trigger primitive electronics) are too slow – some surprises were encountered, e.g. Channel-Link latency about 100 ns (x5 places used)**
  - **How to reach requirement is understood:**
    - ✓ **Optimize data transfer protocols between boards**
    - ✓ **Decrease some bit counts**
    - ✓ **Faster FPGA chips (often 80 MHz versus 40 MHz)**
    - **Improved FPGA algorithms - underway**

Technical Issues (II)

- **DAQ diagnostic readout**
  - **Emu trigger system will store raw data bits**
  - **Useful for debugging to have intermediate trigger calculations:**
    - Input to Sector Receiver: CSC trigger primitives
    - Output of Sector Processor: CSC muon tracks
  - **CMS switched to S-link protocol for DAQ transfer, 200 Mbyte/sec, convenient FIFO output format. We plan to connect to an Ohio State-designed DAQ readout board via optical fiber.**
  - **Concentrator module is needed – 200 Mbyte/sec should be "full"**
- **HDL programming (engineers vs. physicists)**
  - **Present prototype FPGAs use mix of schematics, AHDL**
  - **Would like all FPGAs to be implemented in HDL**
  - **Would like physicists to be able to edit the HDL**

Personnel

- **Professors**
  - Darin Acosta (Florida), Robert Cousins (UCLA), Jay Hauser (UCLA), Paul Padley (Rice)
- **Postdocs**
  - Song Ming Wang (Florida), Benn Tannenbaum (UCLA), Slava Valouev (UCLA)
- **Students**
  - Jason Mumford (UCLA)
- **Engineers**
  - JK (UCLA), Alex Madorsky (Florida), Mike Matveev (Rice), Ted Nussbaum (Rice)
- **Collaborating engineers (all PNPI)**
  - Victor Golovtsov, previously Alex Atamanchuk, Boris Razmyslovich, Vlad Sedov

Conclusions

The CSC muon trigger is now on a firm footing

- ✓ Successful prototyping
- ✓ Full simulation package now available
- ✓ Technical solutions to all problems are known

Plans for future developments are being made

- ❖ We would like support from the review committee for these plans (see Darin/Paul's talks)

Base program cutbacks will/would definitely hurt this project

- CSC trigger requires careful optimization simulation studies by physicists
- Post-docs and students will control the trigger "knobs" that are in FPGAs
- By 2004 (end of Project), engineering support will largely go away